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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,326	03/26/2004	Frank M. Cerio JR.	TAZ-259	9467

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EXAMINER	
MCDONALD, RODNEY GLENN	

ART UNIT	PAPER NUMBER
1795	

NOTIFICATION DATE	DELIVERY MODE
02/17/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/811,326	CERIO ET AL.	
	Examiner	Art Unit	
	Rodney G. McDonald	1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32,33 and 94* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32,33 and 94* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 30, 2009 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 32, 33 and 94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yao et al. (U.S. Pat. 6,051,114) in view of Yasar et al. (US PGPUB. 2003/0034244 A1) and Horii (U.S. Pat. 6,255,177).

Regarding claim 32, Yao et al. teach a method of operating a deposition system comprising positioning a patterned substrate on a wafer table within a processing chamber. The patterned substrate has features such as a field area, a sidewall and a bottom surface. (See Fig. 1; (See Fig. 3A-3C; Column 5 lines 36-43) Creating a high density plasma in the processing chamber wherein the high density plasma comprises ions of coating material and a large number of process gas ions. (Column 3 lines 25-42; Column 6 lines 12-26) Exposing the patterned substrate to the high-density plasma. Performing a Low Net Deposition (LND) process wherein a target and substrate bias power is adjusted to establish an LND deposition rate. (Column 4 lines 7-18; Column 5 lines 44-68; Column 6 lines 1-27) The performing of the LND process step includes depositing material onto the field area at a deposition rate of not more than 30 nanometers per minute while depositing or etching material, or a combination thereof, on the sidewall or the bottom surface or a combination thereof and thereby producing substantially no overhanging material at feature openings. Yao et al. teach controlling parameters to establish a net zero deposition rate on a field area of a substrate. (See Fig. 3B; Column 6 lines 12-27) Yao et al. teach simultaneous bombardment with ions and deposition. (Column 6 lines 12-18)

Regarding claim 33, Yao et al. teach a method of operating a deposition system comprising positioning a patterned substrate on a wafer table within a processing

chamber. The patterned substrate has features such as a field area, a sidewall and a bottom surface. (See Fig. 1; (See Fig. 3A-3C; Column 5 lines 36-43) Creating a high density plasma in the processing chamber wherein the high density plasma comprises ions of coating material and a large number of process gas ions. (Column 3 lines 25-42; Column 6 lines 12-26) Exposing the patterned substrate to the high-density plasma. Performing a Low Net Deposition (LND) process wherein a target and substrate bias power is adjusted to establish an LND deposition rate. (Column 4 lines 7-18; Column 5 lines 44-68; Column 6 lines 1-27) The performing of the LND process step includes depositing material onto the field area at a deposition rate of not more than 30 nanometers per minute while depositing or etching material, or a combination thereof, on the sidewall or the bottom surface or a combination thereof and thereby producing substantially no overhanging material at feature openings. Yao et al. teach controlling parameters to establish a net zero deposition rate on a field area of a substrate. (See Fig. 3B; Column 6 lines 12-27) Yao et al. teach simultaneous bombardment with ions and deposition. (Column 6 lines 12-18)

Regarding claim 94, Yao et al. teach a method of operating a deposition system comprising positioning a patterned substrate on a wafer table within a processing chamber. The patterned substrate has features such as a field area, a sidewall and a bottom surface. (See Fig. 1; (See Fig. 3A-3C; Column 5 lines 36-43) Creating a high density plasma in the processing chamber wherein the high density plasma comprises ions of coating material and a large number of process gas ions. (Column 3 lines 25-42; Column 6 lines 12-26) Exposing the patterned substrate to the high-density plasma.

Performing a Low Net Deposition (LND) process wherein a target and substrate bias power is adjusted to establish an LND deposition rate. (Column 4 lines 7-18; Column 5 lines 44-68; Column 6 lines 1-27) The performing of the LND process step includes depositing material onto the field area at a deposition rate of not more than 30 nanometers per minute while depositing or etching material, or a combination thereof, on the sidewall or the bottom surface or a combination thereof and thereby producing substantially no overhanging material at feature openings. Yao et al. teach controlling parameters to establish a net zero deposition rate on a field area of a substrate. (See Fig. 3B; Column 6 lines 12-27) Yao et al. teach simultaneous bombardment with ions and deposition. (Column 6 lines 12-18) Yao et al. teach depositing a seed layer on the sidewalls of vias or trenches on the substrate. (Figs. 3B, 3C)

The differences between Yao et al. and the present claims is that changing the process from an LND process to a No Net Deposition (NND) process comprising a field deposition rate, a sidewall deposition rate or a bottom surface deposition rate and controlling the chamber conditions to change the process form the LND process to the NND process is not discussed (Claims 32 and 33), the NND process step being used to repair the ruthenium layer is not discussed (Claim 32), the NND process step being used to deposit the ruthenium layer is not discussed (Claim 33) and the seed layer being ruthenium is not discussed (Claim 94).

Regarding claims 32, 33, Yasar et al. teach changing from a LND process to a NND process (i.e. an etching process) by adjusting chamber conditions. (See Paragraph 0035) Yasar et al. suggest depositing a barrier layer and then a seed layer

on a substrate. (See Paragraph 0003; 0004) Yasar et al. suggest utilizing the deposition and etch process to deposit these layers. (See Paragraph 0011)

Regarding the NND process step being used to repair the ruthenium layer (Claim 32), Yasar et al. teach depositing repairing the layer. (See Paragraph 0035) Horii teach depositing a Ru seed layer by sputtering. (Horii et al. Column 6 lines 20-26) Therefore if sputtered in the invention of Yao et al. the Ru would be repaired. (See Yao et al. discussed above)

Regarding the LND process step being used to deposit the ruthenium layer (Claim 33), Horii teach sputtering to produce a Ru layer. Therefore if the Ru was sputtered in the invention of Yao et al. the Ru layer would be deposited. (See Horii Column 6 lines 20-26)

Regarding the seed layer being ruthenium (Claim 94), Horii teach sputtering to produce a Ru seed layer. (Horii Column 6 lines 20-26) Therefore if the Ru was sputtered in the invention of Yao et al. the Ru layer would be deposited. (See Horii Column 6 lines 20-26)

The motivation for utilizing the features of Yasar et al. is that it allows for metallization of high aspect ratio vias. (Paragraph 0002)

The motivation for utilizing the features of Horii is that it allows for forming a seed layer to support further plating metals. (Column 6 lines 61-67; Column 7 lines 1-5)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Yao et al. by utilizing the features of

Yasar et al. and Horii because it allows for metallization of high aspect ratio vias and for forming seed layers to support further plating metals.

Response to Arguments

Applicant's arguments filed November 30, 2009 have been fully considered but they are not persuasive.

In response to the argument that Yao teaches filling of features, it is argued that Yao et al. teach in Fig. 3C a hole that is not completely filled. One of ordinary skill in the art could stop the process at this point in order to produce a hole that is not completely filled. (See Yao discussed above)

In response to the argument that Yao's process is not entirely simultaneous, it is argued that this step comprises etching and depositing since a DC bias is applied. (See Yao discussed above)

In response to the argument that Yasar uses sequential deposition and etching, it is argued that Yasar was relied upon to teach a changing from a LND process to a NND process (i.e. an etching process) by adjusting chamber conditions. (See Paragraph 0035) Yasar et al. suggest depositing a barrier layer and then a seed layer on a substrate. (See Paragraph 0003; 0004) Yasar et al. suggest utilizing the deposition and etch process to deposit these layers. (See Paragraph 0011)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 571-272-1340. The examiner can normally be reached on M-Th with every Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rodney G. McDonald/
Primary Examiner, Art Unit 1795

Rodney G. McDonald
Primary Examiner
Art Unit 1795

RM
February 4, 2010